EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	930	711/152.ccls.	US-PGPUB; USPAT	OR	ON	2008/08/06 14:17
L4	64	("AND" adj gate) and ("OR" adj gate) and L2	US-PGPUB; USPAT	OR	ON	2008/08/06 14:18
L5	33	("AND" adj gate) and ("OR" adj gate) and memory with shar$3 and L2	US-PGPUB; USPAT	OR	ON	2008/08/06 14:25
L7	3	(prevent$3 inhibit$3 repress $3 prohibit$3 preclud$3 mask$3 wait$3) with (peripheral ((external "off chip" off-chip) near2 (processor CPU))) with (access$3 request$3) near4 shar$3 near2 (memory RAM)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/06 15:18
L8	0	(prevent$3 inhibit$3 repress $3 prohibit$3 preclud$3 mask$3 wait$3) with (peripheral ((external "off chip" off-chip) near2 (processor CPU))) with (access$3 request$3) near4 shar$3 near2 (memory RAM)	US-PGPUB; USPAT	OR	ON	2008/08/06 15:20
L9	436	(prevent$3 inhibit$3 repress $3 prohibit$3 preclud$3 mask$3 wait$3) with (peripheral ((external "off chip" off-chip) near2 (processor CPU))) with (access$3 request$3) near4 (memory RAM)	US-PGPUB; USPAT	OR	ON	2008/08/06 15:21
L10	12	(prevent$3 inhibit$3 repress $3 prohibit$3 preclud$3 mask$3 wait$3) with (peripheral ((external "off chip" off-chip) near2 (processor CPU))) with (access$3 request$3) near4 (memory RAM) and shar$3.ti.	US-PGPUB; USPAT	OR	ON	2008/08/06 15:21
L11	214	(peripheral ((external "off chip" off-chip) near2 (processor CPU))) with (access$3 request$3) with memory with (on-chip "on chip")	US-PGPUB; USPAT	OR	ON	2008/08/06 16:00

L12	40	(peripheral ((external "off chip" off-chip) near2 (processor CPU))) with (access$3 request$3) with memory with (on-chip "on chip") and shar$3 near2 memory	US-PGPUB; USPAT	OR	ON	2008/08/06 16:00
L13	126	(peripher$2 ((external$2 "off chip" off-chip outside) near2 (processor CPU))) with (access$3 request$3) with memory near3 (on-chip "on chip" internal) and shar $3 near2 (memory RAM)	US-PGPUB; USPAT	OR	ON	2008/08/06 16:07
L14	13	((external$2 "off chip" off-chip) near2 (processor CPU)) with (access$3 request $3) with memory near3 (on-chip "on chip" internal$2 IC substrate "integrated circuit") and shar$3 near2 (memory RAM) with chip	US-PGPUB; USPAT	OR	ON	2008/08/06 16:09
S3	991	710/36.ccls.	US-PGPUB; USPAT	OR	ON	2007/11/02 13:24
S4	384	710/40.ccls.	US-PGPUB; USPAT	OR	ON	2007/11/02 13:25
S5	1234	710/107.ccls.	US-PGPUB; USPAT	OR	ON	2007/11/02 13:25
S6	171	710/108.ccls.	US-PGPUB; USPAT	OR	ON	2007/11/02 13:27
S7	841	711/152.ccls.	US-PGPUB; USPAT	OR	ON	2007/11/05 14:55
S8	2	("20020007431" "20030115392").pn.	US-PGPUB; USPAT	OR	ON	2007/11/02 14:39
S9	648	710/113.ccls.	US-PGPUB; USPAT	OR	ON	2007/11/02 14:32
S10	511	(peripheral external) near3 processor and (disabl$3 suppress$3) with bus with (request$3 access$3)	US-PGPUB; USPAT	OR	ON	2007/11/02 14:43
S11	176	(peripheral external) near3 processor and (disabl$3 suppress$3) with bus with (request$3 access$3) and "710"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/11/26 11:59
S12	93	(peripheral external) near3 processor and (disabl$3 suppress$3) with bus with (request$3 access$3) with signal and "710"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/11/02 14:44

S13	8	(peripheral external) near3 processor and suppress$3 with bus with (request$3 access$3) with signal and "710"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/11/02 14:44
S14	27	(peripheral external) near3 processor and (mask$3 suppress$3) with bus with (request$3 access$3) with signal and "710"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/11/02 14:45
S15	10	(peripheral external) near3 processor and (mask$3 suppress$3) near4 bus near4 (request$3 access$3) with signal and "710"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/11/26 11:58
S16	13	(peripheral external) near3 processor and (mask$3 suppress$3) near4 bus near4 (request$3 access$3) with signal	US-PGPUB; USPAT	OR	ON	2007/11/02 15:37
S17	51	(mask$3 suppress$3 disabl $3 enabl$3) with "OR" with bus near4 (request$3 access $3) with signal	US-PGPUB; USPAT	OR	ON	2007/11/02 15:38
S18	102	(mask$3 suppress$3 disabl $3 enabl$3) with (logical gate) near2 ("OR" "AND") with bus near4 (request$3 access$3) with signal	US-PGPUB; USPAT	OR	ON	2007/11/02 15:39
S19	79	(mask$3 suppress$3 disabl $3 enabl$3) with (logical gate) near2 ("OR" "AND") with bus near4 (request$3 access$3) with signal and g06f$.ipc.	US-PGPUB; USPAT	OR	ON	2007/11/02 15:42
S20	3	(mask$3 suppress$3 disabl $3 enabl$3) with (logical gate) near2 ("OR" "AND") with bus near4 (request$3 access$3) with signal same (external peripheral off-chip "off chip") and g06f$.ipc.	US-PGPUB; USPAT	OR	ON	2007/11/02 15:42
S21	6430	((first and second) multi multiple plurality plural) with (processor cpu micro $processor controller) with (common shared shar$4) with (bus link channel)	US-PGPUB; USPAT	OR	ON	2007/11/26 10:12

S22	6269	((first and second) multi multiple plurality plural) with (processor cpu micro $processor controller) with (switch mux multiplexer) with (bus link channel)	US-PGPUB; USPAT	OR	ON	2007/11/05 14:57
S23	54	((first and second) multi multiple plurality plural) with (processor cpu micro $processor controller) with (common shared shar$4) with (bus link channel) same (suppress$3 mask$3)	US-PGPUB; USPAT	OR	ON	2007/11/26 10:13
S24	2	shar$3 with bus with master with first near3 request$3 same (disabl$3 standby suppress$3 mask$3)	US-PGPUB; USPAT	OR	ON	2007/11/26 11:30
S25	7	(external peripheral) near2 processor with shar$3 with internal near2 bus	US-PGPUB; USPAT	OR	ON	2007/11/26 11:35
S26	74	external near2 processor with shar$3 with bus	US-PGPUB; USPAT	OR	ON	2007/11/26 11:55
S27	6	external near2 processor with shar$3 with internal near2 bus	US-PGPUB; USPAT	OR	ON	2007/11/26 11:36
S28	72	(external peripher$2) near2 (CPU processor) with (request$3 access$3 shar$3) near4 (internal common) near2 bus	US-PGPUB; USPAT	OR	ON	2007/11/26 11:57
S29	193	peripher$2 with (request$3 access$3 shar$3) near4 (internal common) near2 bus	US-PGPUB; USPAT	OR	ON	2007/11/26 11:57
S30	0	peripheral same (mask$3 suppress$3) near4 bus near4 (request$3 access$3) with signal and "710"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/11/26 11:58
S31	73	peripheral same (disabl$3 suppress$3) with bus with (request$3 access$3) and "710"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/11/26 12:18
S32	30	peripheral same (standby mask$3 suppress$3) with bus with (request$3 access $3) and "710"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/11/26 12:00
S33	90	suppress$3 with bus with request$3	US-PGPUB; USPAT	OR	ON	2007/11/26 13:10
S34	2	suppress$3 with request with bus	EPO	OR	ON	2007/11/27 14:24
S35	47510	@pd<="19850101" and @pd>="19840101"	EPO	OR	ON	2007/11/26 12:26

S36	7299	@pd<="19850101" and @pd>="19841101"	EPO	OR	ON	2007/11/26 12:28
S37	1	"128246".pn.	EPO	OR	ON	2007/11/26 12:27
S38	0	"86601".pn.	EPO	OR	ON	2007/11/26 12:27
S39	912	@pd<="19810101" and @pd>="19801215"	EPO	OR	ON	2007/11/26 12:28
S40	1292	@pd<="19820101" and @pd>="19811215"	EPO	OR	ON	2007/11/26 12:29
S41	1	"42833".pn.	EPO	OR	ON	2007/11/26 12:29
S42	2367	@pd<="19830101" and @pd>="19821215"	EPO	OR	ON	2007/11/26 12:30
S43	635	@pd<="19840101" and @pd>="19831225"	EPO	OR	ON	2007/11/26 12:30
S44	1918	@pd<="19831201" and @pd>="19831120"	EPO	OR	ON	2007/11/26 12:30
S45	946	@pd<="19831201" and @pd>="19831125"	EPO	OR	ON	2007/11/26 12:31
S46	1352	@pd<="19830901" and @pd>="19830825"	EPO	OR	ON	2007/11/26 12:31
S47	927	@pd<="19830901" and @pd>="19830828"	EPO	OR	ON	2007/11/26 12:31
S48	1	@pd<="19830829" and @pd>="19830826"	EPO	OR	ON	2007/11/26 12:32
S49	425	@pd<="19830829" and @pd>="19830825"	EPO	OR	ON	2007/11/26 12:32
S50	869	@pd<="19830830" and @pd>="19830823"	EPO	OR	ON	2007/11/26 12:36
S51	1	"3528062".pn.	US-PGPUB; USPAT	OR	ON	2007/11/26 12:38
S52	0	"0086601".pn.	EPO	OR	ON	2007/11/26 12:38
S53	0	EP0086601.pn.	EPO	OR	ON	2007/11/26 12:38
S54	216	(peripheral "external processor" "external CPU") with (request$3 access$3 shar$3) with internal near2 bus with (processor CPU master)	US-PGPUB; USPAT	OR	ON	2007/11/26 13:11
S55	233	(peripheral "external processor" "external CPU") with (request$3 access$3 shar$3) with internal near2 bus with (processor CPU chip IC "integrated circuit")	US-PGPUB; USPAT	OR	ON	2007/11/26 13:12

S56	56	(peripheral "external processor" "external CPU") near4 (request$3 access$3 shar$3) near3 internal near2 bus	US-PGPUB; USPAT	OR	ON	2007/11/27 11:25
S57	0	disabl$ with (peripheral (external near2 (processor CPU))) with request$3 with (internal shar$3) near2 bus	US-PGPUB; USPAT	OR	ON	2007/11/27 11:26
S58	12	disabl$ with (peripheral (external near2 (processor CPU))) with request$3 near4 bus	US-PGPUB; USPAT	OR	ON	2007/11/27 11:58
S59	43	(off-chip "off chip" near2 (processor CPU)) with request$3 near4 bus	US-PGPUB; USPAT	OR	ON	2007/11/27 14:23
S60	13	("4402044" | "4434462" | "4450519" | "4450524" | "4490785" | "4494193" | "4580216" | "4609985" | "4935894" | "4967390" | "4994963" | "5025412" | "5142625").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/11/27 11:50
S61	30	(prevent$3 inhibit$3 repress $3 prohibit$3 preclud$3) with (peripheral ((external "off chip" off-chip) near2 (processor CPU))) with request$3 near4 bus	US-PGPUB; USPAT	OR	ON	2007/11/27 14:22
S62	0	bus near3 use near3 privelege	US-PGPUB; USPAT	OR	ON	2007/11/27 12:22
S64	2	("20030115392" "20020007431").pn.	US-PGPUB; USPAT	OR	ON	2007/11/27 13:12
S65	28	multiprocessor with single adj program	US-PGPUB; USPAT	OR	ON	2007/11/27 13:12
S66	294	710/309.ccls.	US-PGPUB; USPAT	OR	ON	2007/11/27 14:21
S67	338	710/317.ccls.	US-PGPUB; USPAT	OR	ON	2007/11/27 14:21
S68	6	(prevent$3 inhibit$3 repress $3 prohibit$3 preclud$3) with (peripheral ((external "off chip" off-chip) near2 (processor CPU))) with request$3 near4 bus	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/27 14:23
S69	1	(off-chip "off chip" near2 (processor CPU)) with request$3 near4 bus	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/27 14:23

S70	85	suppress$3 with request with bus	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/27 14:24

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